

Remarks

In the Office action of July 6, 2006, claims 1-7 were allowed. Claims 8-18 were rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter, but were indicated to be otherwise allowable if amended to overcome that rejection.

Independent claim 8 recites a method of performing a mathematical function. To satisfy section 101, the claim must be for a practical application, e.g., where the claimed invention transforms a physical object to a different state or thing, or otherwise produces a useful, concrete and tangible result. Accordingly, Applicants amend claims 8, 9, and 12-14 to recite that the method is carried out "in a parallel multiplier hardware architecture", with the generating of partial products being done "with a gate array of said hardware architecture", the adding of partial products in multiple stages being done with "an addition architecture", and with the sum results being extracted "as outputs" of the addition architecture. Claim 9 specifies that the counting is "by means of a binary counter circuit". As a result of this amendment, there is a physical transformation of the multiplier hardware and its outputs during the course of the method. The method as amended is fully supported by the specification and the steps more closely track the operation of the hardware components set forth in the apparatus claims 1-7. Amended claims 8-14 are now believed to be in condition for allowance.

Conclusion

Applicants thank the Examiner for the indication of allowable subject matter. Reconsideration of the rejection is requested in light of the amendments made herein. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Respectfully submitted,

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